IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (*Currently Amended*) A method of forming damascene pattern in a semiconductor device, the method comprising:

forming an insulating layer on a bottom wiring;

forming via holes that ~~exposing~~ expose a part of the bottom wiring by removing the insulating layer selectively;

filling insides of the via holes to a prescribed thickness using non-conductive material by forming a non-conductive material layer on the insulating layer in which the via holes are formed and selectively removing the non-conductive material layer to expose the insulating layer and allow the non-conductive material to remain for a prescribed thickness;

forming an anti-reflection layer on the via holes and the insulating layer;

forming a mask pattern for trench etching in the insulating layer on which the anti-reflection layer is formed; and

forming a damascene pattern after forming trenches using the mask pattern.

2. (*Cancelled*).

3. (*Currently Amended*) The method of claim ~~2~~ 1, wherein the non-conductive material layer is made of photoresist.

4. (*Currently Amended*) The method of claim ~~2~~ 1, wherein said selective removal utilizes entire surface dry etching process or chemical mechanical polishing process.